CH7525 4 Lane DisplayPort to HDMI Converter

FEATURES

- Compliant with DisplayPort Specification version 1.2a and Embedded DisplayPort (eDP) Specification version 1.3
- Up to 4 Main Link Lanes at either 1.62Gb/s or 2.7Gb/s (HBR) link rate supported
- Support color depth 6/8/10/12bits
- HDMI transmitter compliant with HDMI specification version 1.4b and DVI specification version 1.0
- HDMI transmitter supports up to 300 MHz TMDS clock, and supports up to 3.0Gbps data rate for video timing of 1920x1080@120Hz or 4Kx2K@30Hz
- Supports Enhanced Framing Mode
- Fast and full Link Training for embedded DisplayPort system
- Support eDP Authentication: Alternative Scramble Seed Reset and Alternative Framing
- DisplayPort receiver auto equalization supported for the compensation of input signal attenuation
- Support Spread Spectrum Clocking (de-spreading) for EMI reduction
- HDCP engine compliant with HDCP 1.4 specification with internal HDCP Keys
- On-chip Audio Decoder which support 8 channel Audio input from DP Rx and output from HDMI Tx with sample rate up to 192KHz
- Embedded MCU to handle the control logic
- Support device boot up by loading firmware from On Chip Flash automatically
- Integrated EDID Buffer
- 2 work modes: connect 27MHz crystal, inject 27MHz clock
- DP input detection supported
- Support Auto Power Saving mode and low stand-by current
- DP AUX channel and IIC slave interface are available for firmware update and debug
- Low power architecture
- RoHS compliant and Halogen free package
- HBM 4KV ESD Performance
- Offered in 48-Pin QFN package (6 x 6 mm)

APPLICATION

- Notbook/Ultrabook
- Tablet Device
- Handheld/Portable Device
- DP to HDMI cable
- DP to HDMI Adapter/Docking Station

GENERAL DESCRIPTION

Chrontel's CH7525 is a low-cost, low-power semiconductor device that translates the DisplayPort signal to HDMI/DVI. This innovative DisplayPort receiver with an integrated HDMI Transmitter is specially designed to target the notebook/ultrabook, tablet device and PC market segments. Through the CH7525's advanced decoding / encoding algorithm, the input DisplayPort high-speed serialized multimedia data can be seamlessly converted to HDMI/DVI output.

The CH7525's DP/eDP receiver is compliant with the DisplayPort Specification 1.2a and the Embedded DisplayPort Specification version 1.3. With internal HDCP key Integrated, the device support HDCP 1.4 specifications. In the device's receiver block, which supports four DisplayPort Main Link Lanes input with data rate running at either 1.62Gb/s or 2.7Gb/s, can accept RGB digital formats in either 18 bit or 24-bit, and converted the input signal to HDMI output up to 1920x1080@120Hz or 3840x2160@30Hz. Leveraging the DisplayPort's unique source/sink "Link Training" routine, the CH7525 is capable of instantly bring up the video display to the HDMI/DVI TV/Monitor when the initialization process is completed.

The CH7525 also supports up to 8-channel audio input from DP Rx and output from HDMI Tx with sample rate up to 192 KHz. Available audio bandwidth depends on the pixel clock frequency, the video format timing, and whether or not content protection re-synchronization is needed.

With sophisticated MCU and the On Chip Flash, CH7525 support auto-boot and EDID buffer. Leveraging the firmware auto-loaded from Flash, CH7525 can support DP input detection and determine to enter into Power saving mode automatically.

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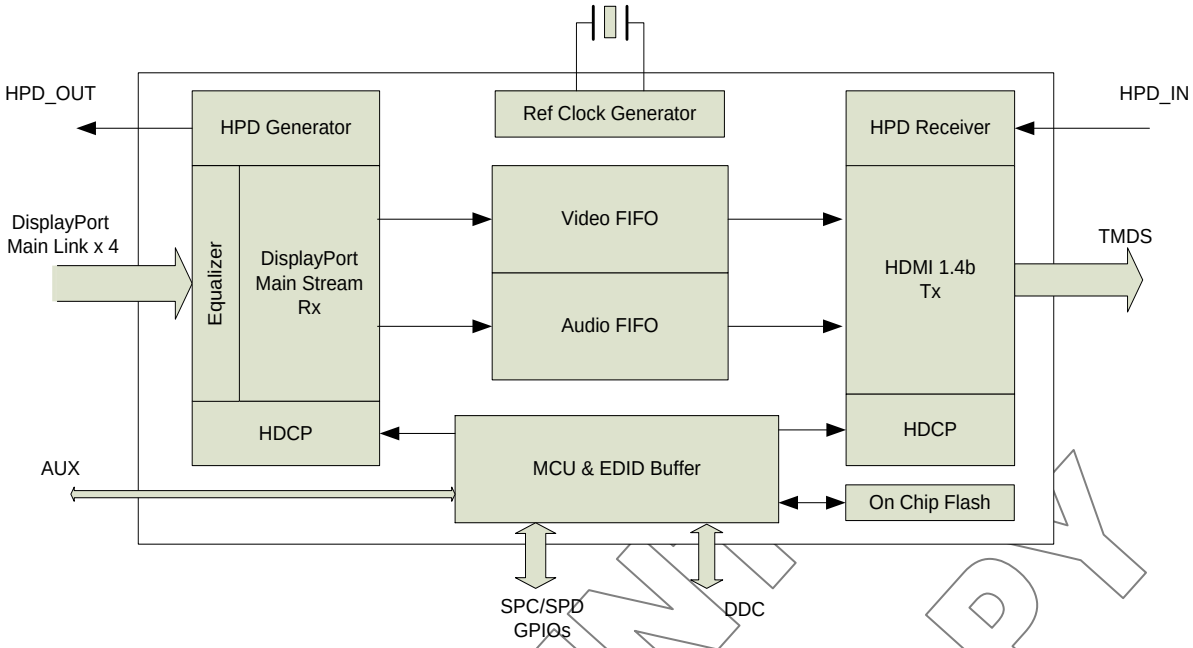

Figure 1: CH7525 Functional Block Diagram

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1.0 PIN-OUT

1.1 Package Diagram

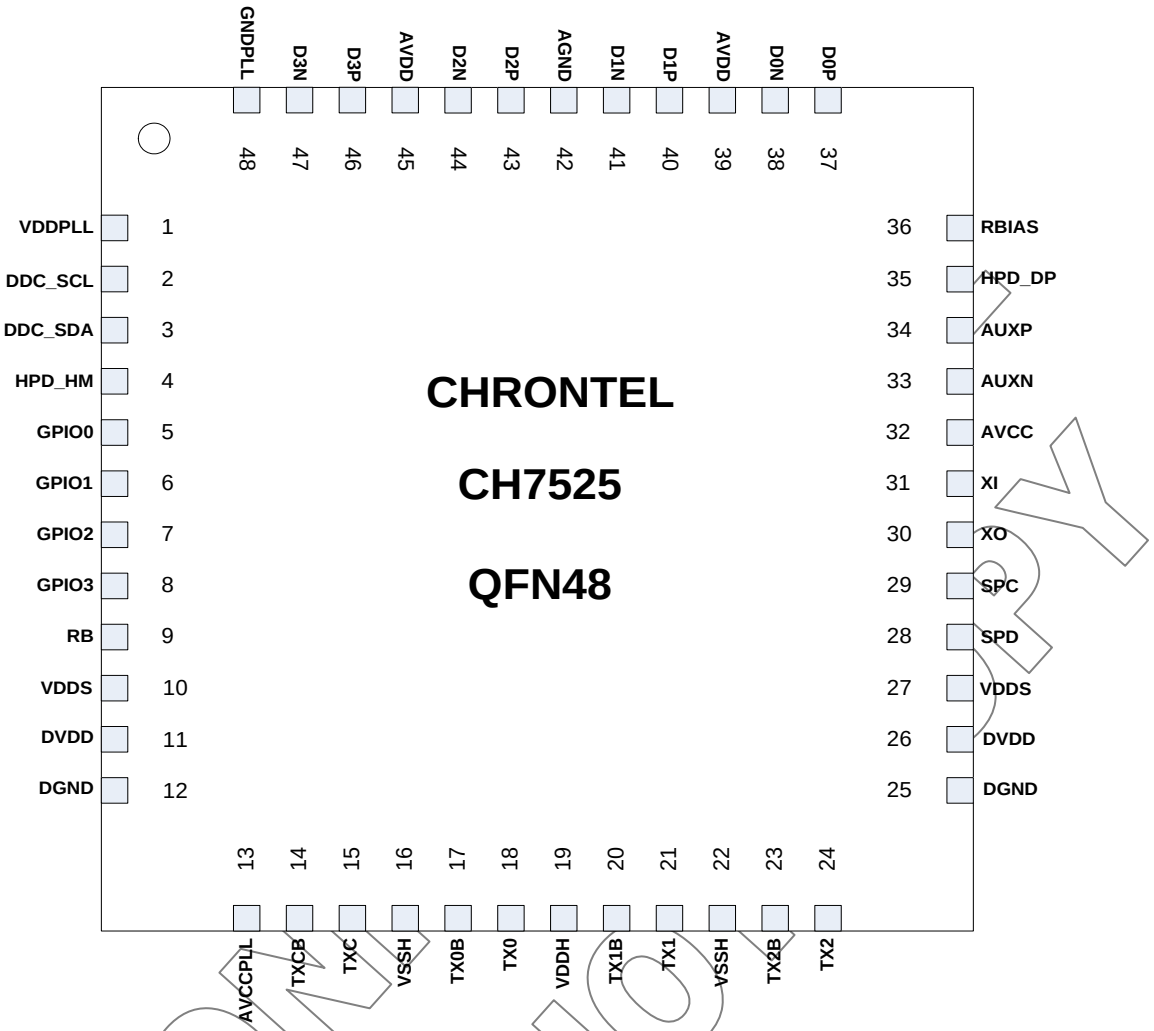

Figure 2: CH7525 48-Pin QFN Pin Out

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1.2 Pin Description

Table 1: Pin Name Descriptions

Pin #	Type	Symbol	Description
2	Out	DDC_SCL	**Serial Port Clock Output to HDMI Receiver** The pin should be connected to clock signal of HDMI DDC. This pin requires a pull-up 1.8 kΩ resistor to the desired voltage level
3	In/Out	DDC_SDA	**Serial Port Data to HDMI Receiver** The pin should be connected to data signal of HDMI DDC. This pin requires a pull-up 1.8 kΩ resistor to the desired voltage level
4	In	HPD_HM	**HDMI Transmitter Hot Plug Input**
5~8	In/Out	GPIO[3:0]	**General Purpose Input/Output**
9	In	RB	**Reset* Input (Internal pull-up)** When this pin is low, the device is held in the power-on reset condition. When this pin is high, reset is controlled through the serial port register.
14,15	Out	TXCB,TXC	**HDMI Tx Clock Outputs** These pins provide the differential clock output for the DVI .
17,18	Out	TX0B,TX0	**HDMI Tx Data Channel 0 Outputs** These pins provide the TMDS differential outputs for data channel 0
20,21	Out	TX1B,TX1	**HDMI Tx Data Channel 1 Outputs** These pins provide the TMDS differential outputs for data channel 1
23,24	Out	TX2B,TX2	H**DMI Tx Data Channel 2 Outputs** These pins provide the TMDS differential outputs for data channel 2
28	In/out	SPD	**Serial Port Data Input / Output** This pin functions as the bi-directional data pin of the serial port. External pull-up 6.8 KΩ resister is required
29	In	SPC	**Serial Port Clock Input** This pin functions as the clock pin of the serial port. External pull-up 6.8 KΩ resister is required
30	Out	XO	**Crystal Output** A parallel resonance crystal should be attached between this pin and XI / FIN. However, if an external CMOS clock is attached to XI/FIN, XO should be left open
31	In	XI	**Crystal Input / External Reference Input** A parallel resonance crystal should be attached between this pin and XO. However, an external 3.3V CMOS compatible clock can drive the XI Input
33,34	In/Out	AUXP, AUXN	**AUX Channel Differential Input/Output** These two pins are DisplayPort AUX Channel control, which supports a half-duplex, bi-directional AC-coupled differential signal.
35	Out	HPD_DP	**DP Receiver Hot Plug Output**
36	Input	RBIAS	**Current Set Resistor Input** This pin sets the basic current for internal circuit. A 10KΩ, 1% tolerance resistor should be connected between this pin and AVSS using short and wide traces
37,38,40, 41,43,44, 46,47	In	D[3:0]P/N	**DP Main Link Differential Line Input** These pins accept four AC-coupled differential pairs signals from the DisplayPort transmitter.
1	Power	VDDPLL	**PLL Power Supply (1.2V)**
10,27	Power	VDDS	**Digital Serializer Power Supply (1.2V)**
11,26	Power	DVDD	**Digital Core/IO Power Supply (1.2V)**
12,25	Power	DGND	**Digital Ground**

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13	Power	AVCCPLL	**PLL Power Supply (3.3V)**
16,22	Power	VSSH	**HDMI Tx Ground**
19	Power	VDDH	**HDMI Tx Power Supply (3.3V)**
32	Power	AVCC	**Analog Power Supply (3.3V)**
39,45	Power	AVDD	**Analog Power Supply (1.2V)**
42, Thermal Pad	Power	AGND	**Analog Ground**
48	Power	GNDPLL	**PLL Ground**

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2.0 PACKAGE DIMENSION

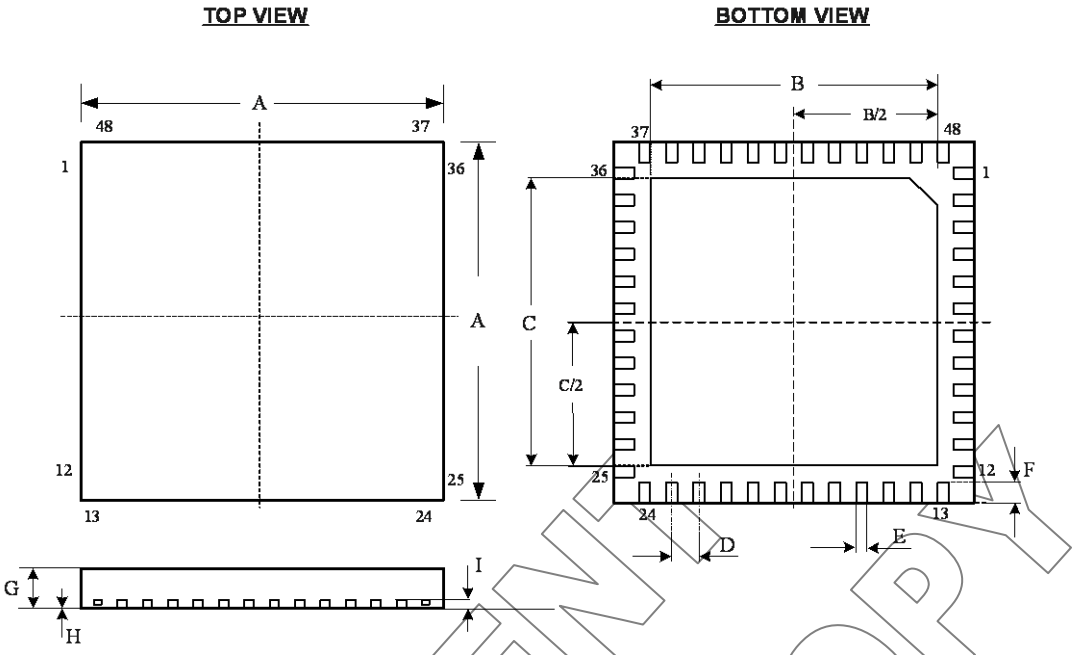

Figure 3: 48 Pin QFN Package

Table of Dimensions

No. of Leads		SYMBOL								
48 (6 X 6 mm)		A	B	C	D	E	F	G	H	I
Milli-meters	MIN	5.90	4.35	4.35	0.4	0.13	0.30	0.70	0	0.20
	NOM	6.00	4.50	4.50		0.19	0.40	0.75	-	-
	MAX	6.10	4.65	4.65		0.25	0.50	0.80	0.05	0.203

Notes:
Conforms to JEDEC standard JESD-30 MO-220.

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ORDERING INFORMATION

Part Number	Package Type	Content Protection	Operating Temperature Range	Minimum Order Quantity
CH7525A-BF	48 QFN, Lead-free	None	Commercial : 0 to 70°C	**490/Tray**
CH7525A-BFK	48 QFN, Lead-free	HDCP 1.4	Commercial : 0 to 70°C	**490/Tray**
CH7525A-BFI	48 QFN, Lead-free	None	Commercial : -40 to 85°C	**490/Tray**
CH7525A-BFIK	48 QFN, Lead-free	HDCP 1.4	Commercial : -40 to 85°C	**490/Tray**

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